

IN THE CLAIMS

Please amend the claims to the following.

1. (Currently Amended) An apparatus comprising:
a trigger-response mechanism that includes at least one bank of user-programmable registers to identify a user-defined trigger event; and
a thread switch handler coupled to the trigger-response mechanism, the thread switch handler to invoke a second instruction stream responsive to an indication from the trigger-response mechanism that the a user-defined trigger event has occurred during execution of a first instruction stream.
2. (Currently Amended) The apparatus of claim 1, wherein the user-defined trigger event includes a synchronous user-defined trigger event, and wherein the thread switch handler is further to invoke the second instruction stream responsive to an indication from the trigger-response mechanism that the a synchronous user-defined trigger event has occurred during execution of the first instruction stream.
3. (Currently Amended) The apparatus of claim 1, wherein the user-defined trigger event includes an asynchronous user-defined trigger event, and wherein the thread switch handler is further to invoke the second instruction stream responsive to an indication from the trigger-response mechanism that the an asynchronous user-defined trigger event has occurred during execution of the first instruction stream.

1 4. (Original) The apparatus of claim 1, wherein the thread switch handler is to save
2 an instruction pointer address for the first instruction stream before invoking the
3 second instruction stream.

1 5. (Original) The apparatus of claim 4, further comprising: a task queue to receive
2 the instruction pointer address.

3 6. (Original) The apparatus of claim 5, wherein: the task queue further comprises a
4 memory location.

5 7. (Original) The apparatus of claim 5, wherein: the task queue further comprises a
6 register.

7 8. (Original) The apparatus of claim 1, further comprising: a plurality of event
8 counters coupled to the trigger-response mechanism, wherein each event counter
9 is to detect an atomic processor event.

1 9. (Currently Amended) The apparatus of claim 8, wherein the user-defined trigger
2 event includes an asynchronous trigger event based on one or more of the atomic
3 processor events, and wherein the thread switch handler is further to invoke the
4 second instruction stream responsive to an indication from the trigger-response
5 mechanism that the an asynchronous user-defined trigger event has occurred
6 during execution of the first instruction stream; ~~wherein the asynchronous user-~~
7 ~~defined trigger event is based on one or more of the atomic processor events.~~

8 10. (Original) The apparatus of claim 1, wherein the thread switch handler is to save
9 context information for the first instruction stream before invoking the second
10 instruction stream.

11 11. (Original) The apparatus of claim 10, wherein: the thread switch handler is further
12 to save context for the first instruction stream in a memory location before
13 invoking the second instruction stream.

14 12. (Original) The apparatus of claim 10, wherein: the thread switch handler is further
15 to save context for the first instruction stream in a register before invoking the
16 second instruction stream.

1 13. (Currently Amended) The apparatus of claim 1, further comprising:
2 one or more user-programmable control registers coupled to the thread switch handler;
3 the value of the one or more control registers to indicate a the weight of context
4 information for the first instruction stream to be saved responsive to invoking the second
5 instruction stream.

1 14. (Currently Amended) A system comprising:
2 a memory to hold ~~store~~ an instruction; and
3 a ~~single-threaded~~ processor coupled to the memory, ~~wherein the processor~~ including
4 ~~provides a thread context; wherein the processor includes a trigger-response mechanism~~ raw
5 event detection logic to detect at least one raw event, a user-addressable register to specify a
6 user-defined trigger event based on the at least one raw event, and ~~to detect a user-specified~~
7 ~~trigger event and also includes~~ a switch handler to invoke a helper thread responsive to
8 occurrence of the user-defined trigger event.

1 15. (Currently Amended) The system of claim 14, wherein: the instruction includes a
2 marking instruction, when executed, to specify the user-defined trigger event in
3 the user-addressable register. ~~the memory is a DRAM.~~

1 16. (Currently Amended) The system of claim 14, wherein: the instruction is a trigger
2 instruction; and raw event detection logic is to the trigger-response mechanism is
3 ~~further~~ to detect an ~~the~~ opcode of the trigger instruction when the trigger
4 instruction reaches an execution phase of an execution pipeline.

1 17. (Currently Amended) The system of claim 14, wherein: the processor further
2 includes a user-addressable control register to specify a weight of a context to be
3 saved responsive to invoking the helper thread.
4 ~~the instruction is a marking instruction that specifies the trigger event, the trigger event~~
5 ~~being asynchronous; and the trigger-response mechanism is further to detect the~~
6 ~~asynchronous trigger event.~~

1 18. (Original) The system of claim 14, wherein: the switch handler is further to
2 maintain minimal context information for a current thread before invoking the
3 helper thread, wherein the minimal context information excludes traditional
4 context information.

1 19. (Original) The system of claim 18, wherein: the excluded traditional context
2 information further comprises general register values.

1 20. (Original) The system of claim 18, wherein the minimal thread context
2 information comprises an instruction pointer address value.

1 21. (Original) A method comprising:
2 detecting a user-specified trigger condition;
3 suspending execution of a first thread on a single-threaded processor;
4 utilizing hardware to save minimal context information for the current thread without
5 operating system intervention; and
6 invoking a second thread on the single-threaded processor without operating system
7 intervention.

1 22. (Original) The method of claim 21, wherein:
2 detecting a user-specified trigger condition further comprises determining that a trigger
3 instruction has been encountered.

1 23. (Original) The method of claim 21, wherein:
2 detecting a user-specified trigger condition further comprises determining that an
3 asynchronous condition specified in a marking instruction has been encountered.

1 24. (Original) The method of claim 21, wherein:
2 utilizing hardware to save minimal context information further comprises saving an
3 instruction pointer address value.

1 25. (Currently Amended) The method of claim 21, further comprising:
2 determining that the first thread should be resumed[[]];
3 restoring the minimal context information for the first thread; and
4 resuming execution of the first thread without operating system intervention.

1 26. (Original) The method of claim 21, wherein detecting a user-specified trigger
2 condition further comprises:
3 receiving a marker instruction that specifies the trigger condition; and
4 monitoring a plurality of atomic event indicators to detect the trigger condition.

1 27. (Original) The method of claim 21, wherein detecting a user-specified trigger
2 condition further comprises:
3 generating an asynchronous response to indicate that the second thread should be invoked.

1 28. (New) A processor comprising:
2 event detection logic to detect a raw event;
3 user-programmable event logic coupled to the event detection logic to indicate a user-
4 defined trigger event, the user-defined trigger event to be based on at least the
5 raw event;
6 user-programmable context control logic to specify a weight of a context to be saved;
7 and
8 thread switch logic coupled to the user-programmable event logic and context control
9 logic, the thread switch logic, in response the user-defined trigger event being
10 detected, to save a portion of a first context based on the weight of a context to
11 be saved that is to be specified in the user-programmable context control logic
12 and to spawn a helper thread without operating system intervention.

1 29. (New) The system of claim 28, wherein the user-programmable event logic
2 includes at least a user-programmable event register, and wherein the user-
3 defined trigger event is to be programmed in the user-programmable event
4 register in response to execution of a user marking instruction.

1 30. (New) The system of claim 28, further comprising trigger response logic coupled
2 to the user-programmable event logic and the event detection logic to detect the
3 user-defined trigger event based on at least the raw event, wherein the trigger
4 response logic is to monitor for the user-defined trigger event for a predetermined
5 timeout period after execution of the user-marking instruction.